INVESTIGATING SINGLE EVENT LATCHUP PHENOMENON IN COMMERCIAL ANALOG-TO-DIGITAL CONVERTERS FOR SPACE APPLICATIONS: EXPERIMENTAL STUDY, TRIGGERING MECHANISMS, AND TESTING CONSIDERATIONS

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ABSTRACT

On-board electronics play a crucial role in the operation and control of spacecraft, enabling navigation, communication, and data processing. As the space electronics application domain is exponentially growing due to the exponentially growing satellite industry, the radiation effects on electronic devices become the primary concern for creating the radiation rated electronics supply chain. Space-based components essentially means radiation hardened circuitry, which has to be rigorously tested to make sure the circuit works as intended without disruption during the lifetime of the mission. However, testing capacity in aerospace is an ongoing challenge, with only a few facilities in the world offering single-event effects testing; which is one of the primary ways of radiation hardness assurance testing of microelectronic devices and integrated circuits. By collaborating with TI and MSU FRIB, we explored both technical and methodological ways of testing analog-to-digital (ADC) integrated circuits using relativistic heavy ion beam and UV-flash-light-photoemission microscopy. The main objective was to understand the single-event latchup (SEL) phenomenon, assess its impact and effects on the performance parameters of ADCs, determine SEL susceptibility, and identify specific areas within ADC architectures that are most prone to SEL.

ACKNOWLEDGEMENTS

First and foremost, I would like to extend my deepest gratitude to my parents for their unwavering love, support, and faith in me. Their belief in the endless potential for progress and their tireless efforts in providing me with opportunities they themselves never had are the foundation upon which my accomplishments stand.

I am incredibly thankful and humbled to have had the privilege of being guided by two exceptional teachers and mentors, Professor Sergey Baryshev and Ram Gooty. The knowledge, wisdom, and passion they have imparted upon me have been truly transformative in my life. I consider myself fortunate to have had the opportunity to study and work under their tutelage, as their expertise has consistently inspired me to strive for greatness and realize how much more there is to learn.

In referring to Mr. Baryshev and Mr. Gooty as not only teachers but also mentors, I aim to emphasize the invaluable human connections they have forged with me. Their genuine concern for my well-being and growth, both professionally and personally, has been reminiscent of the nurturing bond my late grandfather, a distinguished professor himself, shared with his former academic advisor, who eventually became an esteemed academician. This profound example of human relationships and the almost paternal care I have experienced while being away from my homeland and family is an indelible and precious memory that I will forever cherish.

In conclusion, I would like to reiterate my deepest appreciation to my parents, Professor Baryshev, and Ram Gooty for their unwavering support, guidance, and encouragement. Their presence in my life has played an instrumental role in shaping the person I am today, and their impact will continue to resonate as I embark on new challenges and endeavors in the future.

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LIST OF ABBREVIATIONS

SEE Single Event Effects

SEL Single Event Latchup

IC Integrated Circuit

CMOS Complementary Metal Oxide Semiconductor

UV Ultra-Violet

EMMI Emission Microscopy

PEM Photon Emission Microscopy

INTRODUCTION

Semiconductor devices and systems, including integrated circuits (ICs), are vital components in various modern high-tech applications. However, their functionality can be compromised when exposed to different types of radiation found in both natural and man-made environments. This thesis aims to investigate the impact of radiation on semiconductor devices, particularly focusing on single event latchup (SEL) effects, and provide additional insights into triggering mechanisms, and considerations into testing procedures.

The radiation types of concern in this research include heavy ions and UV photons as these types can ionize the material they pass through, generating excessive charge (electron-hole pairs) that may interfere with normal device operation. There are numerous physical mechanisms by which functionality may be degraded. These mechanisms manifest as failure modes, which are broadly classified into two categories: total dose effects and single event effects (SEEs). Total dose effects typically result in parametric degradation due to charge generated in insulating materials, while SEEs are triggered by charge generated in the semiconductor from a single particle strike. SEEs can be further categorized as soft or hard device errors. Soft errors temporarily disrupt device functionality and can be cleared via re-sets, whereas hard errors can cause structural damage, potentially permanently disabling a device. SEL is a prominent hard error that occurs in widely-used CMOS IC technology due to the presence of the core p-n-p-n structures, also known as thyristors, during the fabrication process [1],[2]. Narrowing the scope of this research further, the thesis focuses on hard SEE/SEL effects in digital IC's using heavy ion beam at FRIB and UV flash light combined with emission microscopy (EMMI).

This study is conducted in partnership with Texas Instruments, a leading provider of IC's for space applications, to develop a general testing methodology for devices intended for

commercial space products and applications. Additionally, collaboration with MSU FRIB, which operates a particle accelerator facility, allows for the testing devices in simulated space radiation environments, particularly when exposed to heavy ions. The primary device under investigation in this thesis is an Analog-to-Digital-Converter (ADC), an electronic component that converts analog signals into digital signals. ADCs are crucial in a wide range of applications, such as telecommunications, medical imaging, military, and aerospace systems. Various types of ADCs are available, including flash ADCs, integrating ADCs, sigma-delta ADCs, and successive approximation ADCs. This research employs a high-power superconducting linear accelerator (linac) test method from MSU FRIB and a superconducting cyclotron and an advanced electron cyclotron resonance (ECR) ion source test method from TAMU Cyclotron Radiation Effects Facility, as well as flash test method, primarily focusing on an ADCs provided by Texas Instruments

BACKGROUND

Let us now delve into various applications of electronics in space environments. First and foremost, on-board electronics play a crucial role in the operation and control of spacecraft, enabling navigation, communication, and data processing. Aviation electronic systems (avionics), too, is essential for the functioning of space vehicles, as it ensures the proper management of various systems, such as propulsion, life support, and power distribution. Satellite navigation systems like GLONASS and GPS have become integral to our daily lives, thanks to their utilization of electronic components. These systems facilitate accurate positioning and timing information for a wide range of applications, including transportation, agriculture, and emergency response services.

Ionizing radiation from outer space encompasses a variety of factors that can significantly impact spacecraft and their electronic components. One of the main sources of radiation is the Earth's radiation belts or so called Van Allen Belts (shown in Fig.1), which are regions where charged particles, primarily protons and electrons, are trapped by the planet's magnetic field. These particles can adversely affect the electronic equipment on spacecraft, leading to functional and parametric failures, ultimately compromising the performance and reliability of the systems [3].

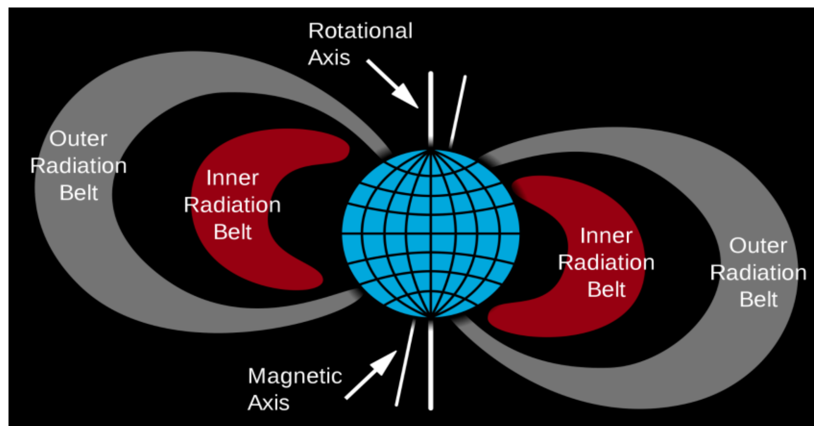


Figure.1: Van Allen Radiation Belts.

A second source of radiation exposure in space, particularly in the near-Earth orbit, is the solar flares. Solar flares are powerful bursts of energy from the Sun that produce effects on electronic components similar to those produced by the Van Allen Belts. However, solar flares are more challenging to manage, as predicting solar activity is almost impossible to predicted. Even when solar activity can be accurately forecasted, it remains difficult to determine the direction and intensity of a specific flare, as well as the actual radiation levels at the location of a satellite or spacecraft [4].

Last but not least, there are heavy charged particles or so called heavy ions that can acutely affect electronics operation. Heavy ions consist of the atomic nuclei of heavy elements with high atomic mass and number (>20), and originate from the depths of our galaxy. Upon colliding with the delicate crystals comprising microelectronic circuits in spacecraft systems, these heavy charged particles can induce single-event effects (SEEs) [5]. SEEs encompass a range of phenomena that can cause functional failures in space electronic equipment.

All known space radiation effects can be broadly categorized into two groups: dose effects and single-event effects. Each of the two categories is associated with distinctly different sources of the radiation and different electronic system malfunction consequences. Dose effects primarily result from the radiation emitted by the Earth's radiation belts and solar flares. Over time, the accumulated radiation dose can lead to degradation in the performance of electronic components and materials, potentially causing system malfunctions or failures. Therefore, dose effects pose significant challenges for the long-term operation and reliability of spacecraft electronics. Single-event effects occur in semiconductor devices due to bombardment by heavy ions. These effects encompass a range of phenomena, from temporary disruptions like single-event upsets to

permanent damages such as the single-event latchup and burnout. Single-event effects, therefore, pose serious risks to the functionality and integrity of space electronic equipment, necessitating the development of mitigation strategies and radiation-hardened components [6].

Giving it a closer look, dose effects primarily occur in semiconductor structures, particularly at the interface between silicon and oxide layers. For instance, consider a cross-section of a bipolar device of an integrated circuit, where the oxide layer is situated above the semiconductor structure.

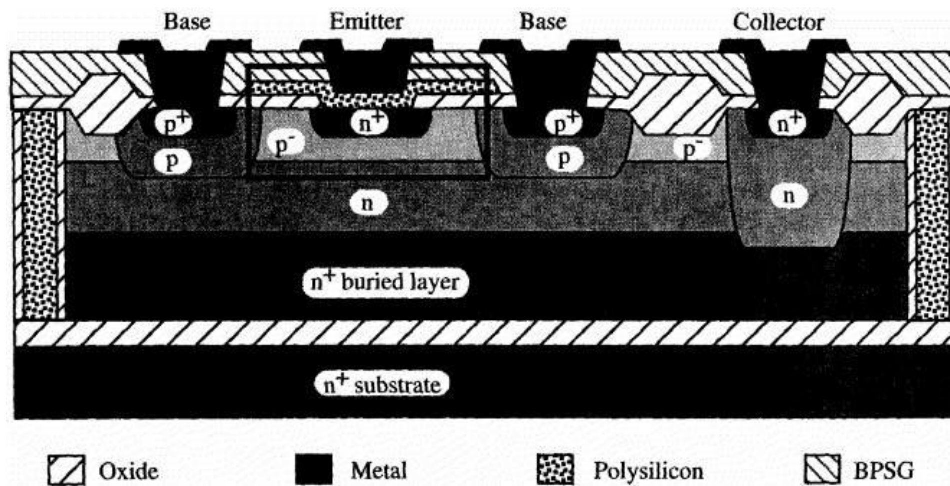


Figure 2: Schematic cross-section of a n-p-n bipolar structure. The base oxide is of most interest to bipolar ionizing radiation response, and is shown by the hatched region that overlies the p-region of the base.

When exposed to radiation, ionization process cascades take place. During ionization, electron-hole pairs are generated. At a given applied voltage, electrons possess higher mobility, ionization results in the accumulation of positive charge within the oxide layer due to holes being less mobile. Over time, this accumulated charge transforms into surface states or defects at the interface between silicon and oxide layers, negatively impacting the characteristics of semiconductor devices [7]. This series of processes is shown schematically in Fig.3. The accumulation of charge

in the oxide not only affects bipolar structures but also influences the properties of MOS (metal-oxide-semiconductor) structures, which form the basis of the contemporary digital electronics. These effects can lead to a shift in threshold voltages and performance degradation due to changes in the operating point (volt-ampere characteristics' steepness). If trapped charges in the oxide turn into surface states, surface recombination increases thereby hurting the performance of semiconductor devices even further [8]. In bipolar transistors and large scale IC's, radiation effects lead to a decrease in the gain. Fig. 4 shows a plot tracking the decrease a BJT gain as a function of accumulated dose. In MOS structures, the accumulation of charge in the gate oxide results in shifted threshold voltage levels thereby changing the gain and switching threshold in logic gates. All these effects are irreversible.

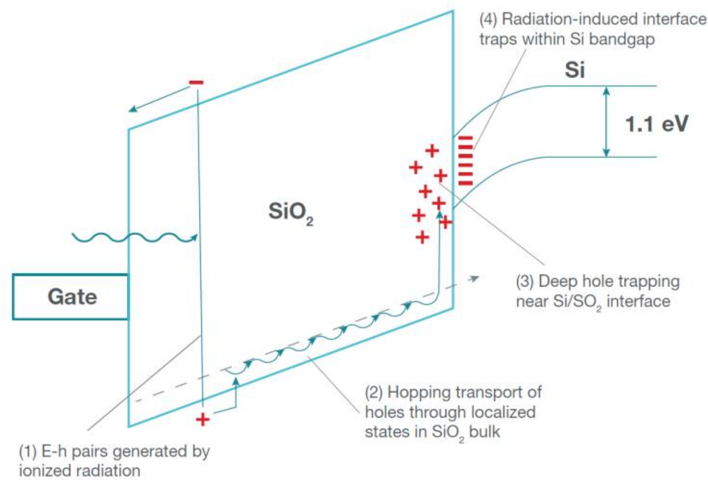


Figure 3: Band diagram of a MOS device with positive gate bias showing the effect of ionizing radiation on carrier generation, transport and trapping [8].

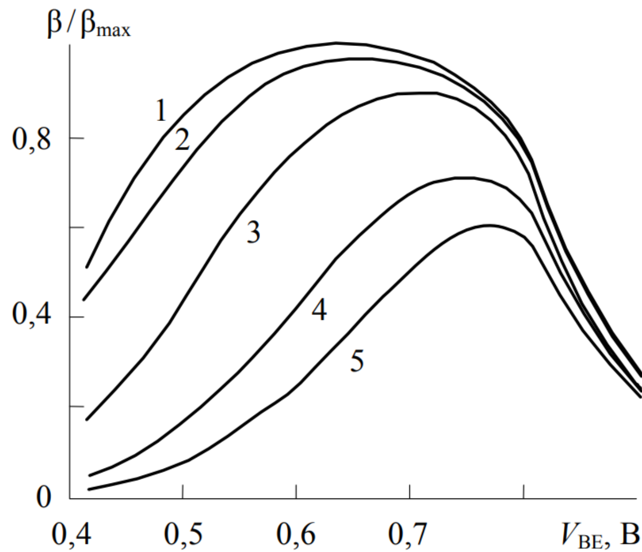


Figure 4: Dependence of the gain of a BJT on the bias-emitter forward bias for various radiation doses measured in Gray [Gy]: 1 - 0; 2 - 100; 3 - 500; 4 - 2000; 5 – 5000.

SEEs, on the other hand, occur in ICs due to the impact of heavy ions. While the dose yield for these particles is generally not substantial, they cause instantaneous localized ionization. This localized ionization, in turn, leads to the generation of electron-hole pairs in specific regions of the semiconductor circuit. When a substantial charge is generated and separated by an internal electric field, such as a reverse-biased p-n junction, it produces a significant localized ionization current spike. This current often causes switching events, for example, upsets in memory cells. The distortion of information stored in a memory is a consequence of such SEEs. It is obvious, the greater the heavy ion flux, the greater the frequency of upsets and distortions, the less likely those failures can be effectively corrected using methods like checksums or parity bits. This can escalate from a single event failure to a functional failure of the entire electronic device. Additionally, SEEs encompass the thyristor effect, thereby posing a significant problem. When a particle penetrates a sensitive area, a parasitic p-n-p-n structure is activated, causing a substantial current to flow between the power input and the ground. This often results in microcircuit burn-outs. Essentially,

heavy ion irradiation lead to both functional and parametric failures of the microcircuit, which cannot be restored even through corrective measures.

The single event latchup (SEL) is a well-known hard error type, particularly because it is a ubiquitous error in the complementary metal-oxide-semiconductor (CMOS) technology [1, 2]. When manufacturing CMOS circuits using bulk technology, it is impossible to avoid the formation of p-n-p-n structures, which are also referred to as thyristors. Fig.5 illustrates one such parasitic structure that arises due to the side-by-side placement of NMOS and PMOS transistors. This latchup can happen in the device because of the presence of a parasitic p-n-p transistor and a parasitic n-p-n transistor, both of which are connected in a feedback loop. The parasitic p-n-p transistor is formed by the p+ source, n-well, and p-substrate, while the parasitic n-p-n transistor is formed by the n+ source, p-substrate, and n-well. The overlaid equivalent circuit demonstrates that the output (collector) of each transistor is connected to the input (base) of the other transistor. If a transient current is introduced into the device, either through circuit conditions or because of an ion strike, the feedback loop can amplify this current and cause it to sustain itself. The high current state that emerges is exactly the latchup. It ceases to exist only the dc power is removed or if the device is destroyed by the high current density [10, 11].

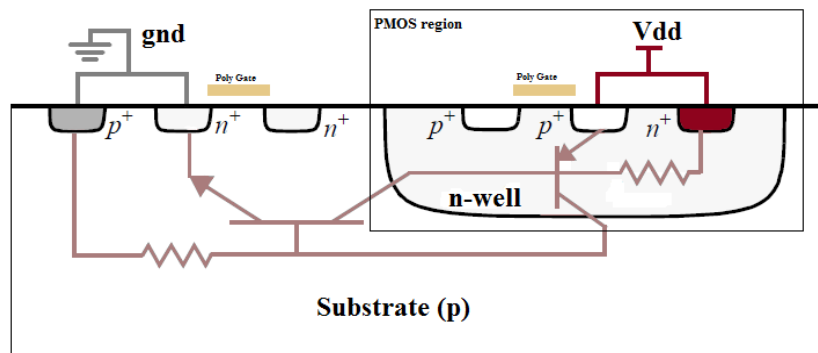


Figure 5: Simplified cross section of a CMOS inverter stage with NMOS (left) and PMOS (right) transistors. The parasitic p-n-p and n-p-n bipolar transistors are the cause of latchups when a positive feedback is formed.

ICs can experience latchup due to electrical conditions or radiation environment. Despite the distinct ways these stimuli initiate latchup, once triggered steady-state conditions for latchup become the same [1]. For instance, the holding voltage and holding current, which are the minimum conditions necessary to maintain latchup, remain independent of the triggering method. As a consequence, many electrical latchup hardening strategies can also be applied to SEL [2]. However, electrical and radiation stimuli do not affect identical regions of an IC. Electrical latchup tends to occur near the Input/Output (I/O) terminals [1]. These I/O terminals are susceptible to receiving hazardous electrical signals, while the core circuitry is situated in a more controlled and safer environment. Due to this, the semiconductor industry focuses on applying latchup mitigation strategies primarily to the I/O circuitry and aims to make the core circuitry as dense as possible. On the other hand, a heavy ion can pass through any region of an IC, leading SEL to occur in the core circuitry, where small n+ to p+ source spacings are utilized. Consequently, SEL mitigation strategies must be applied across the entire IC, thereby significantly increasing the area and decreasing the overall performance of ICs.

Latchup susceptibility of ICs depend on a wide range of process, layout, and environmental parameters [12], which makes it challenging to predict the susceptibility of a specific IC to latchup and to determine the most effective mitigation strategy. Nevertheless, the simplified circuit depicted in Fig.5 can be utilized to understand how latchup susceptibility is influenced by operating conditions and structural alterations in the p-n-p-n region. The feedback loop in Fig.5 comprises cross-coupled parasitic p-n-p and n-p-n bipolar junction transistors (BJTs) and decoupling resistors. Under normal bias conditions, the parasitic BJTs conduct minimal current, and regenerative feedback does not take place in this loop. However, when the BJTs are triggered into the forward-active mode, they cause significant current conduction and regenerative feedback,

introducing a low impedance path between the supply voltage (Vdd) and the ground. As depicted in Fig.5, the base/collector junction of both BJTs (i.e., the n-well/p-substrate junction) is reverse biased under normal conditions. Therefore, to trigger the two BJTs into the forward-active mode, it is only necessary to forward bias their emitter/base junctions, which correspond to the source/body junctions of the MOSFETs. The n+ and p+ sources are directly connected to the power rails and are heavily doped, ensuring that their potentials remain fixed. On the other hand, the bodies of the NMOS and PMOS transistors in Fig.5 are biased through the substrate and n-well resistances, respectively. These resistances shunt the emitter/base junctions of the p-n-p and n-p-n transistors. Consequently, potential drops across these resistances causing the emitter/base junctions to be forward biased. If a triggering event forward biases only one of these two junctions, the corresponding BJT enters the forward-active mode and forces current through the base resistance of the other BJT. This action can cause the other BJT to also enter the forward-biased mode, thereby establishing latchup.[16]

An increase in operating temperature also promotes latchup for several reasons: higher temperatures reduce the potential needed to turn on the emitter/base junctions of the parasitic BJTs, increase bipolar amplification, and increase the resistances that shunt the emitter/base junctions and hence the dissipated power [13]. Additionally, an increase in supply voltage (Vdd) promotes latchup. As shown in Fig.5, Vdd is applied across the collector-emitter regions of both BJTs. In other words, Vce and Vec is equal to Vdd for the n-p-n and p-n-p transistors. If a charged particle strike generates a specific amount of current in the base of the n-p-n transistor, the transistor will produce a collector (output) current with a magnitude determined by Vce (=Vdd). Consequently, larger supply voltages lead to larger collector currents, making it easier for one BJT to trigger the other into the forward-active mode, thereby establishing latchup. A larger supply voltage is also

more likely to exceed the holding voltage compared to a smaller one, making it more probable that latchup is sustained and cause damage.

Normal electrical latchup and single event latchup are two distinct phenomena that can occur in semiconductor devices, particularly in CMOS structures. While both latchup types can lead to device malfunction or failure, they have different causes and mechanisms. Some detailed comparison between normal latchup and SEL are as follows

Normal Latchup:

Cause: Normal latchup is typically triggered by electrical disturbances, such as voltage spikes, current transients, over-voltage, or excessive input current. It can also occur due to process variations or design flaws.

Mechanism: Unintended turn-on of parasitic BJTs in CMOS structures that creates low-impedance paths between the power supply rails. High current flows and causes excessive heat and may cause device degradations and burn-outs.

Prevention: Additional protection is used such as guard rings, substrate biasing, engineering the substrate resistivity, and silicon-on-insulator (SOI) or deep trench isolation.

Detection: Normal latchup can be detected using I-V curve tracing or power supply input power real time tracking.

Single Event Latchup:

Cause: SEL is caused by high-energy ionizing particles striking a sensitive region of the device.

Mechanism: Heavy ion passing through creates (stochastically) localized current transients, called single event transient (SET). If the SET occurs in the base region of the parasitic BJTs, it can turn them on thereby triggering a latchup.

Prevention: Prevention radiation-hardening techniques are used such as radiation-tolerant shielding materials and layout optimization, circuit-level error-correcting codes, watchdog timers, or auxiliary circuitry.

Detection: SEL can be detected in operando by real-time input power tracking. Ex situ photon emission microscopy (PEM) is often used to localize the failing area within the circuitry after the SEL occurs.

In order to minimize the likelihood of functional and parametric failures, integrated circuits designed for space applications must undergo rigorous radiation testing. These tests are conducted in various simulation facilities, including installations with isotope sources of gamma radiation such as Co-60 for dose effects testing. Such experiments are performed in research institutes and testing centers worldwide, as this issue is of significant importance and has attracted considerable attention. Tests for SEEs are carried out at particle accelerators, where digital and analog integrated circuits are examined for failure effects under the influence of heavy charged particles and accelerated ions of various chemical elements like argon, xenon, and many more. During radiation testing NI rack hardware run on LabVIEW is used to measure radiation effects in real time at high rates while controlling and monitoring the temperature and counting and recording the actual events.

It is essential to understand that when launching a commercial satellite, cost constraints must be taken into consideration. Utilizing special-purpose microcircuits, which have been designed with all necessary radiation protection measures, can be quite costly for those involved in commercial space projects. As an alternative, commercial microelectronic products can be used, provided that they undergo the comprehensive radiation tests mentioned previously. This approach

can help strike a balance between cost-effectiveness and reliability in the demanding environment of space applications.

Physical inspection methods, including reverse engineering, electrical and optical probing, photonic emission analysis, fault injection techniques, and side-channel analysis, have been developed and deployed to assist in the failure analysis (FA). FA tools such as chip polishing, microscopy, focused ion beam, X-ray imaging, and laser voltage probing have undergone significant advancements to support these techniques. The need for higher yields and more expedited FA and fault localization at increasingly smaller technology nodes has also driven the development and innovation of FA methods and tools. Physical inspection can be categorized into non-invasive, semi-invasive, and invasive methods. In recent years, despite the addition of new features, FA equipment has become more affordable and easily accessible. Our focus is on semi-invasive inspection/attack. Semi-invasive attacks occupy the middle ground between non-invasive and invasive attacks. These types of attacks were first employed to flip a bit in a microcontroller SRAM cell using a photoflash lamp [14]. When a target transistor is illuminated, it causes the transistor to conduct, which in turn induces a transient fault. These types of attacks are not only practical but also affordable, as they do not necessitate costly laser equipment. For example, these attacks have been successfully executed using a $30 flashgun purchased second-hand from a camera store [14]. Similar to invasive attacks, semi-invasive attacks require that the chip under test is unpackaged in order to access the chip surface. However, the passivation layer of the chip remains intact, as semi-invasive methods do not require electrical contact with the metal surface, thus avoiding mechanical damage to the chip. In theory, semi-invasive attacks could be performed using tools such as UV light, X-rays, lasers, electromagnetic fields, and localized heating, either

individually or in combination. Despite this, the field of semi-invasive attacks has not been extensively explored.

With the ongoing trend towards smaller and more densely packaged ICs, the susceptibility of microelectronic devices to SELs is increasing, necessitating the development of effective detection and mitigation techniques. In this thesis, we evaluate ADC ICs by combining photon emission microscopy (PEM) and in *operando* radiation testing at the relativistic ion cyclotron FRIB. These techniques are complimentary in that they provide real time data on radiation hardness of commercial ICs with high spatial resolution localization of malfunction points.

OBJECTIVE OVERVIEW, EXPERIMENTAL SETUP, RESULTS & DISCUSSIONS

The following experimental tests aim to provide an understanding of the SEL phenomenon in ADCs. Exploring the reasons behind the occurrence of single event latch-up includes frequency of occurrence (or how often SELs happen), impact of SEL on circuit behavior, and very importantly occurrence locations of SELs within ADCs (localization of the failure). Elaborating upon previous discussion of how energetic particle attacks can create localized transient currents and voltages, thereby triggering the parasitic thyristor effect, we describe the impact on circuit performance as the increase in current flow and risks of component damage, malfunction or failure. We characterize ADCs via studying SELs induced by the effects of heavy ion and UV flashlight irradiation. When applied to the same ADC, heavy ion and UV light radiation could potentially serve as complementary means to study *in operando* real-time SEL detection and tracking while allowing for localizing SELs within studied circuits. The following TI ADC were studied:

- ADS131M08, 24-bit delta-sigma (ΔΣ) ADC tested by heavy-ion irradiation. Heavy-ions with an LET_{EFF} of 75 MeV-cm^2/mg were used to irradiate the devices with a fluence of 1×10^7 ions/cm^2 at MSU FRIB facility.
- ADS9818 high-speed, 18-bit SAR ADC tested by UV photon irradiation/PEM for i.e. failure localization.
- ADS8168, 16-bit SAR ADC tested by both heavy-ion irradiation and UV photon/PEM for failure localization after heavy-ion exposure. Heavy-ions with an LET_{EFF} of 48 MeV-cm^2/mg were used to irradiate the devices with a fluence of 1×10^7 ions/cm^2 at TAMU facility.

The CMOS process node is used in nearly all modern ADCs from TI. Therefore, we hypothesized that the thyristor effect would be the main effect to track in real time testing at

cyclotron facilities. The main signature of the thyristor effect excess is the current injection through parasitic bipolar structure leading to power and ground contacts latching until the power is removed/reset or until the device is destroyed by high current. The methodology to detect and track the SELs is to monitor the current and voltage at the power source I/O. The results demonstrated that ADS131M08 failed at LET_{EFF} = 75 MeV-cm^2/mg at 125 °C. Similarly, ADS8168 failed at LET_{EFF} = 48 MeV-cm^2/mg at 85 °C. As latchup testing must be performed at the highest device operating temperature which is stated in MIL-STD-883-1

ADS131M08

Device and Test Board Information

The ADS131M08 is an eight-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, low power, and energy-measurement-specific features, making the device an excellent fit for energy metering, power metrology, and circuit breaker applications in space. The ADC inputs can be directly interfaced to a resistor-divider network or a power transformer to measure voltage or to a current transformer or a Rogowski coil to measure current. ADS131M08 is packaged in a 32-pin plastic package as shown in Fig. 7. The ADS131M08EVM evaluation module was used to evaluate the performance and characteristics of the ADS131M08 under heavy-ion irradiation tests. Fig. 8 shows the top view of the evaluation board with the de-capped tested chip used for the radiation testing.

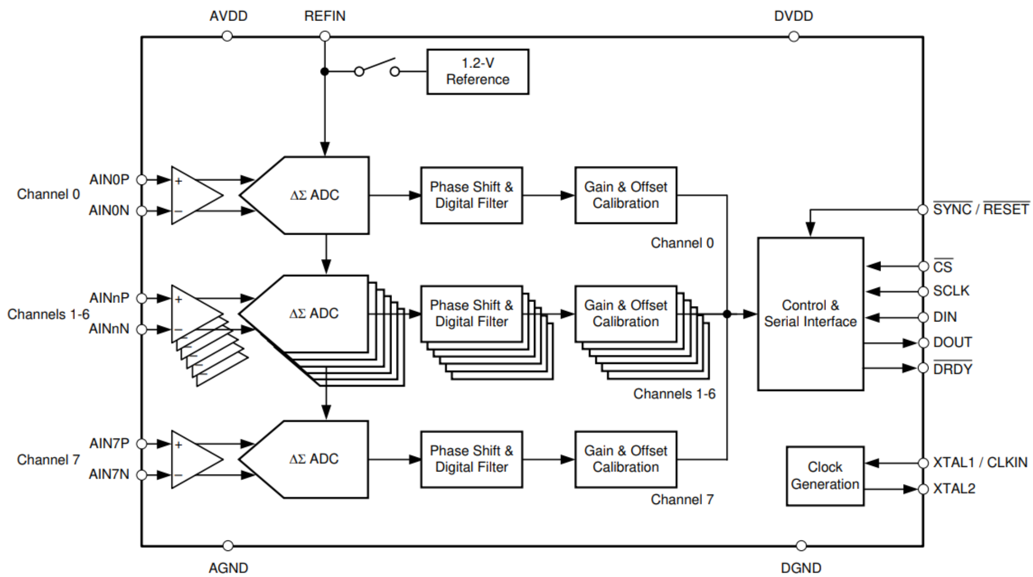
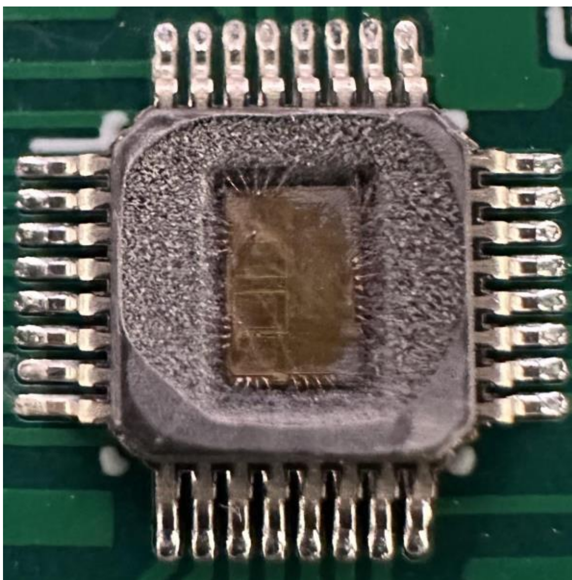


Figure 6: Functional block diagram of the ADS131M08.



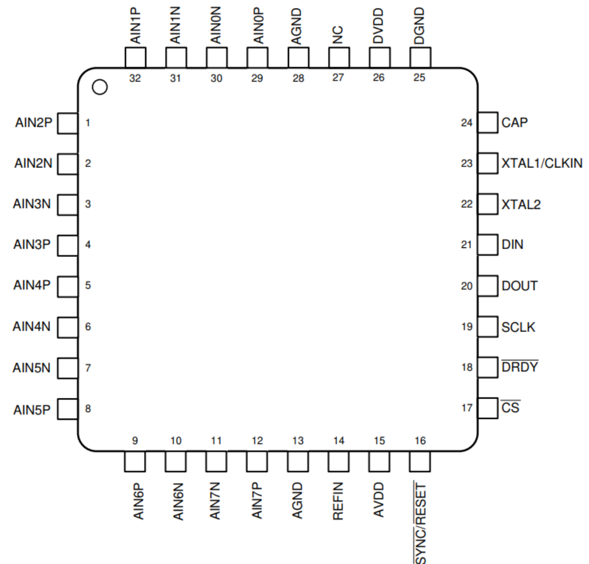


Figure 7: Photograph of de-capped ADS131M08 [Left] and its pin configuration [Right].

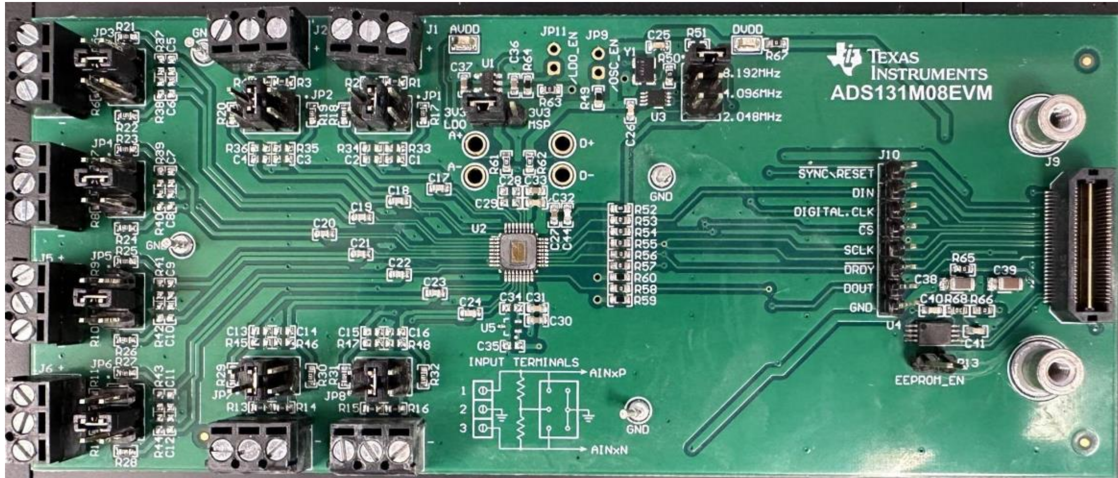


Figure 8: ADS131M08EVM board top view.

The ADS131M08EVM eases the evaluation of the device with hardware, software, and computer connectivity through a USB interface. The evaluation kit includes the ADS131M08EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis. The ADS131M08EVM board includes the ADS131M08 ADC and all the peripheral analog circuits and components required to drive and track performance of the ADC. The PHI board primarily serves three functions:

1) Provides a communication interface from the EVM to the computer through a USB port.

2) Provides the digital input and output signals necessary to communicate with the ADS131M08.

3) Supplies power to all active circuitry on the ADS131M08EVM board.

The ADS131M08 evaluation module kit that is shown on the picture above has the following features:

1) Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS131M08 ADC.

2) No external power supply is required (USB powered.)

3) The PHI controller provides communication interface to the ADS131M08 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output.

4) Runs under 64-bit Microsoft Windows 7, 8, and 10.

5) The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

Fig. 10 illustrates an example system setup for evaluation.

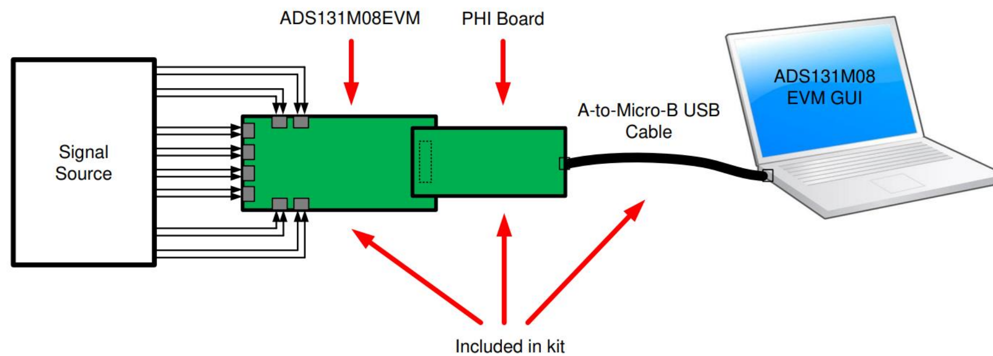


Figure 9: System connection for evaluation.

Most importantly for our FRIB and TAMU tests, the GUI ADS131M08EVM of provides us with the time domain display tool, allowing for visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS131M08EVM, as per the current interface mode settings indicated in Fig. 10 by using the capture button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage.

Figure 10: Time domain display tool options.

Irradiation Facility and Setup

This product was tested at the Michigan State University Facility for Rare Isotope Beams (MSU FRIB) using a cutting-edge cyclotron accelerator. Throughout the majority of these studies, ion flux of 10^5 ions/s-cm^2 was used in order to provide heavy ion fluence of 10^7 ions/cm^2. For these experiments, Thulium (Tm) ions were utilized. Fig. 11 shows the installation/testing set up for ADS131M08EVM at MSU FRIB. The in-air gap between the device and the ion beam port window was maintained at 70 mm for all runs.

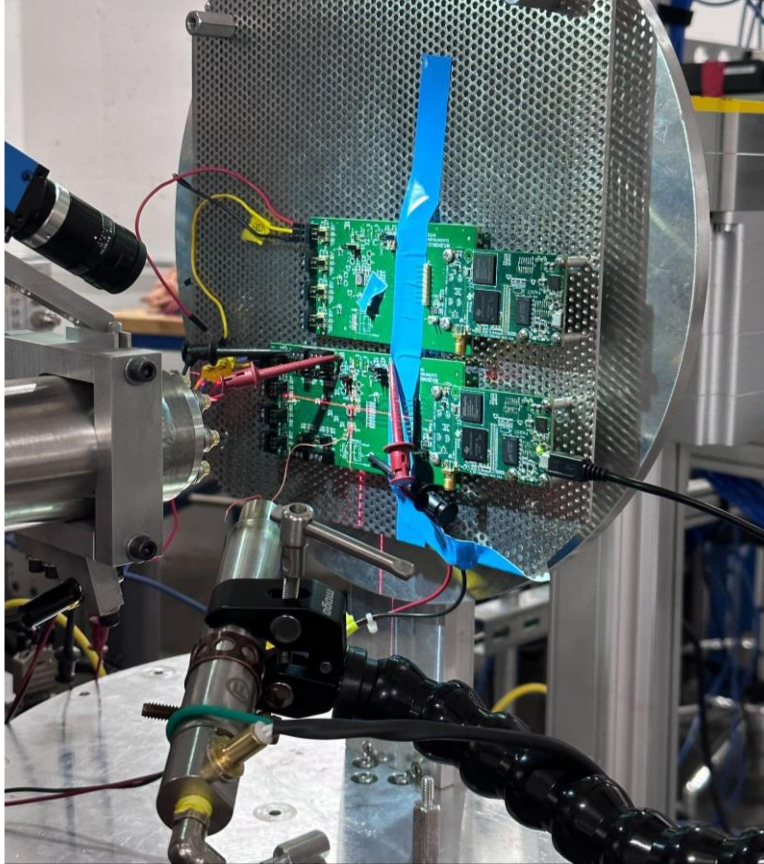


Figure 11: Photograph of the ADS131M08EVM mounted in front of the heavy-ion beam exit port at MSU FRIB end user station.

Single-Event Latchup Results and Discussion

During SEL characterization the device was heated and maintained at temperature 125 °C with steady flow from a heat gun maintaining the device. The temperature was monitored using an IR-camera. Thulium isotope ^{169}Tm ions were utilized for the SEL testing, with an angle-of-incidence of 0°, resulting in an effective linear energy transfer (LET_{EFF}) of 75 MeV-cm^2/mg. A flux of roughly 10^5 ions/s-cm^2 and a fluence of 10^7 ions/cm^2 were employed for three separate runs. The voltage supply for V_A and V_D was provided externally on board, with the highest recommended voltage setting of 3.6 V. The supplied current to the device from the power supply was constantly monitored through a LabView GUI. Table 1 illustrates that SEL events were

observed during all three runs. Additionally, Fig. 12 presents a plot of the power supply current versus time detecting and tracking the latchup events.

Table 1: ADS131M08 SEL Conditions Using ^{169}Tm at an Angle-of-incidence of 0°.

RUN #	**DISTANCE (mm)**	**TEMPERATURE (°C)**	**ION**	**ANGLE**	**FLUX (ions×cm²/mg)**	**FLUENCE (# of ions)**	**LET_{EFF} (MeV×cm²/mg)**
1	70	125	Tm	0°	1.00E+05	1.00E+07	75
2	70	125	Tm	0°	1.00E+05	1.00E+07	75
3	70	125	Tm	0°	1.00E+05	1.00E+07	75

AVDD	DVDD	AINP	AINM (GND)	Expected output code	I_{AVDD} Actual	I_{DVDD} Actual	I_{VREF} actual	Actual Output Code
3.6	3.6	0.6V	0	0.6V	7mA	5.6mA	<1mA	1V
3.6	3.6	1.2V	0	0.6V	7mA	5.6mA	<1mA	0.6V
3.6	3.6	1.2V	0	0.6V	7mA	5.6mA	<1mA	0.6V

Comments	Results	Notes about the device
AVDD latched up, reset didnt help to recover and can not capture. Device recover after power cycle and can capture. Transients appear through the run	FAIL	internal ref @1.2V. External toggled through the register
Clamp change 250mA, AVDD latch up, RESET didn't help to recover and can not capture. Device recover after power cycle and can capture	FAIL	internal ref @1.2V. External toggled through the register
Clamp change 250mA, AVDD latch up,no continuous capture	FAIL	internal ref @1.2V. External toggled through the register

ADS131M08 was reset in one of three ways: 1) by a power-on reset (POR), 2) by SYNC/RESET pin, or 3) by a RESET command. After a reset occurs, the configuration registers are reset to the default values and the device begins generating conversion data as soon as a valid MCLK (Master Clock) is provided.

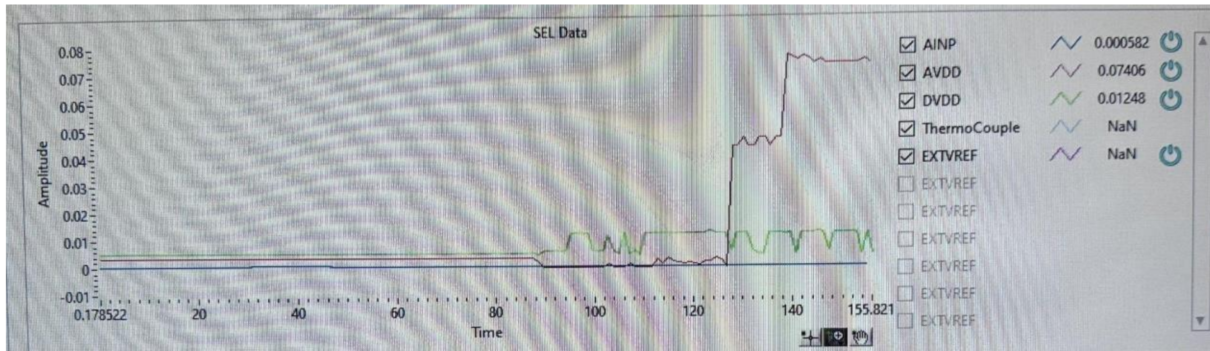


Figure 12: Current vs time (I vs t) tracking data for Vs current during SEL Run #3.

SEL was observed, indicating that the ADS131M08 is prone to SELs at (and hence above) LET_{EFF}=75 MeV-cm^2/mg and T = 125°C. In conducting an experimental test, we sought to gain an understanding of the circuit's response to SEL occurrences. Analysis of the results, as illustrated in Fig. 12 and Fig. 13, provides valuable insights into the circuit's behavior during SEL events. Approximately 40 seconds following the initiation of the particle beam, a notable increase in the AVDD (Power Supply for the analog portion of the IC) current was observed, peaking at 74 mA. This elevated current level persisted until a power cycling intervention was executed by power-on reset to restore normal operation. Subsequently, it was discovered that ADC experienced a latchup, which in turn led to erratic and unreliable ADC conversions as can be seen in real time in Fig. 13. These results provided us with initial ideas of the ADC's behavior under heavy ion beam, as well as with understanding of functional operation during SEL occurrence.

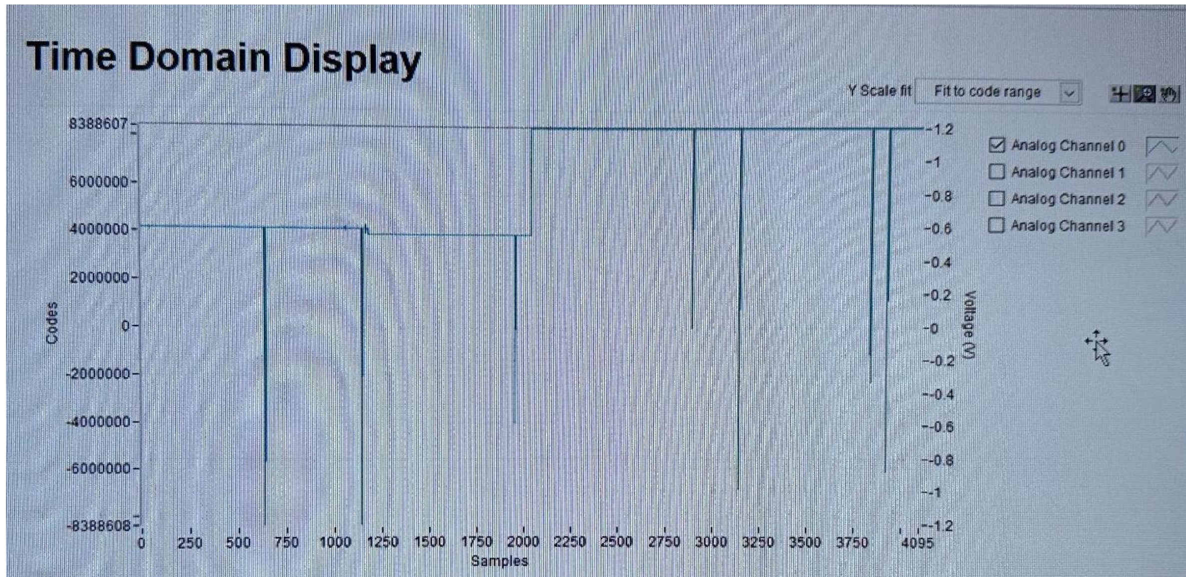


Figure 13: Time Domain Display of the ADS131M08 during SEL event.

The SEL cross-section measured at the maximum LET was calculated to be $\sigma_{SEL} = 1.25\times10^{-6}$ cm^2. A cross-section in this context is a measure of the probability of an SEE occurring and is expressed in terms of area cm^2. The SEL cross-section represents the probability that a single energetic particle (ion) will cause a latch-up event when it strikes the device. In other words, it characterizes the susceptibility of the device to radiation-induced latch-up events. It provides a quantitative measure of how likely the device is to experience a latch-up event when exposed to a specific radiation environment. So, the calculated cross-section of 1.25×10^{-6} cm^2 implies that every millionth (approximately) ion strike will cause a latchup. The details on how SEL cross-section was calculated are given in Appendix A. Finally, it was conclusively determined that the ADS131M08 ADC is susceptible to SELs at 75 MeV/cm^2-s and hence is not suitable for space applications as it does not pass a baseline requirement described in MIL-STANDARD 883-1.

With this new insight into the ADC's response to SEL events, the next interest was to try localize SEL events on the tested chip, in other words identify the areas within the circuit that are

most susceptible to SEL. To do this, we used photoemission microscope where latchups are activated by a UV flash light attack. The next ADC was therefore tested using complementary cyclotron and PEM tools that took heavy ion and UV photon radiation as the means to induce latchups.

ADS9818

Device and Test Board Information

The ADS9818 is an eight-channel data acquisition (DAQ) system based on a dual, simultaneous sampling, 18-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADS9818 features a complete analog front-end for each channel with an input clamp, 1-MΩ input impedance, independently programmable gain amplifier (PGA), programmable low-pass filter, and an ADC input driver. The device also features a low-drift, precision reference with a buffer to drive the ADCs. A high-speed digital interface supporting 1.2-V to 1.8-V operation enables the ADS9818 to be used with a variety of host controllers. ADS9818 is packaged in a 56-pin plastic package as shown in Fig. 15. The ADS9818EVM evaluation module was used to evaluate the performance and characteristics of the ADS9818 under high energy UV flashlight. Fig. 16 shows the top view of the chip under test.

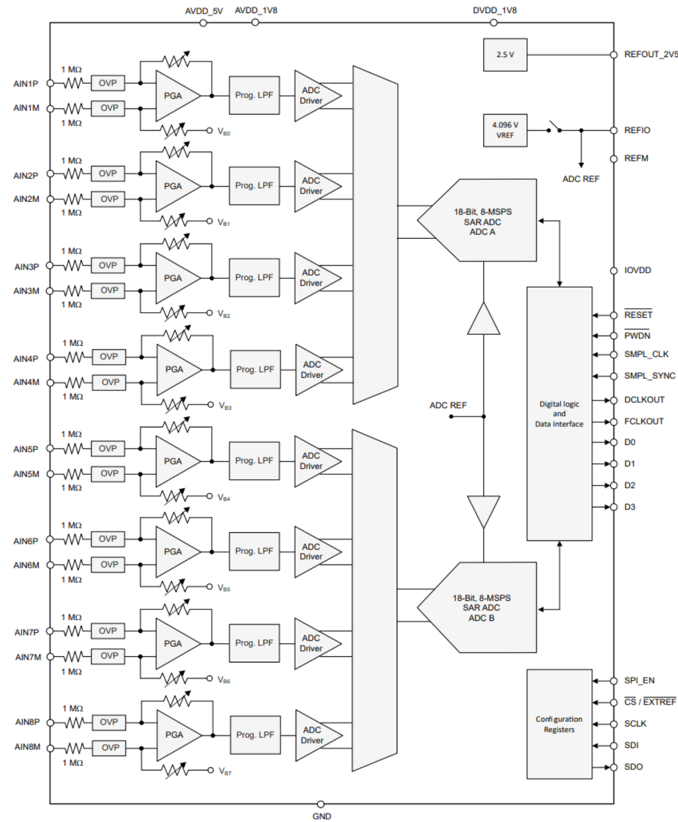


Figure 14: Functional Block Diagram of the ADS9818.

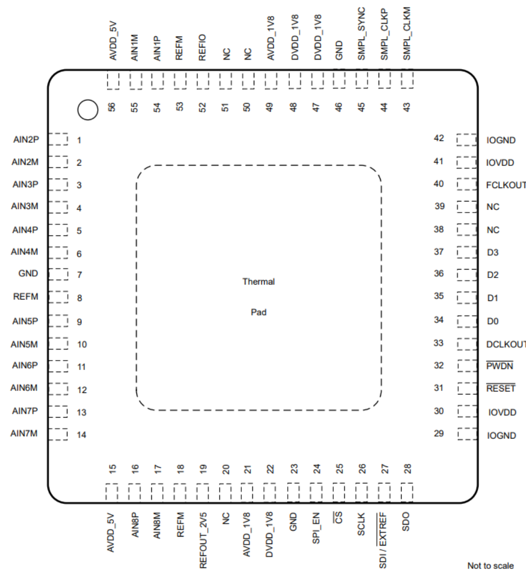


Figure 15: ADS9818 pin configuration

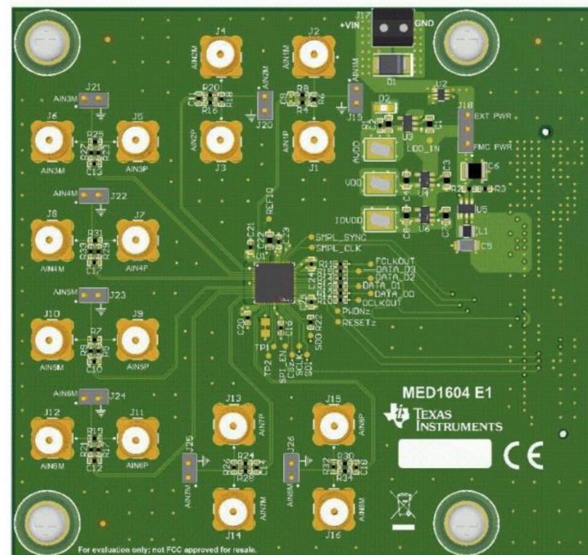


Figure 16: ADS9818EVM board top view

Testing Facility and Setup

The high energy photons used for the SEE studies on this product were studied at Texas Instruments. High energy photons were delivered from a halogen flashlamp. Photon-emission microscopy tool (PEM, also known as emission microscopy dubbed as EMMI) a Hamamatsu Phemos 1000 was used. PEM utilizes the effect of photons emitted whenever an electron/hole pair recombines – a photon with wavelength anywhere between 350 nm and 1100 nm is emitted. PEM utilizes a highly sensitive detector to collect these photons and integrates the signal over time in order to generate an image of the emission "hot spots" that is later overlaid on top of the optical image of the DUT. In this experiment, the Si-CCD detector camera was used. Fig. 17 shows the ADS9818EVM tested device, high energy flashlamp, and Phemos 1000 used for the experiments.

Figure 17: Photograph of the ADS9818 latchup replication test setup.

Latchup Replication Results and Discussion

During the characterization of the latchup replication, the device was tested at room temperature. Primary UV photons were utilized to trigger latchups. The voltage supply for VA and VD was provided externally on board, with the highest recommended voltage setting of 5.5 V and 1.8 V respectively. Table 2 illustrates that the latchup event was observed. Additionally, Fig. 18 shows images of the hot spots, providing details of the localization of the latchups across the internal structure of the device. By replicating the latchup state with a high-power UV flashlamp on the ADS9818 device, we were able to cause the V_{DD} current to reach an elevated state of 54 mA.

Table 2: Power Supply currents during Latch-up replication test.

Device Status	AVDD (5.5V)	IOVDD (1.8V)	VDD (1.8V)
Power Up Current	21 mA	11 mA	19 mA
After Configuration	40 mA	20 mA	43 mA
Post Flash	40 mA	20 mA	54 mA

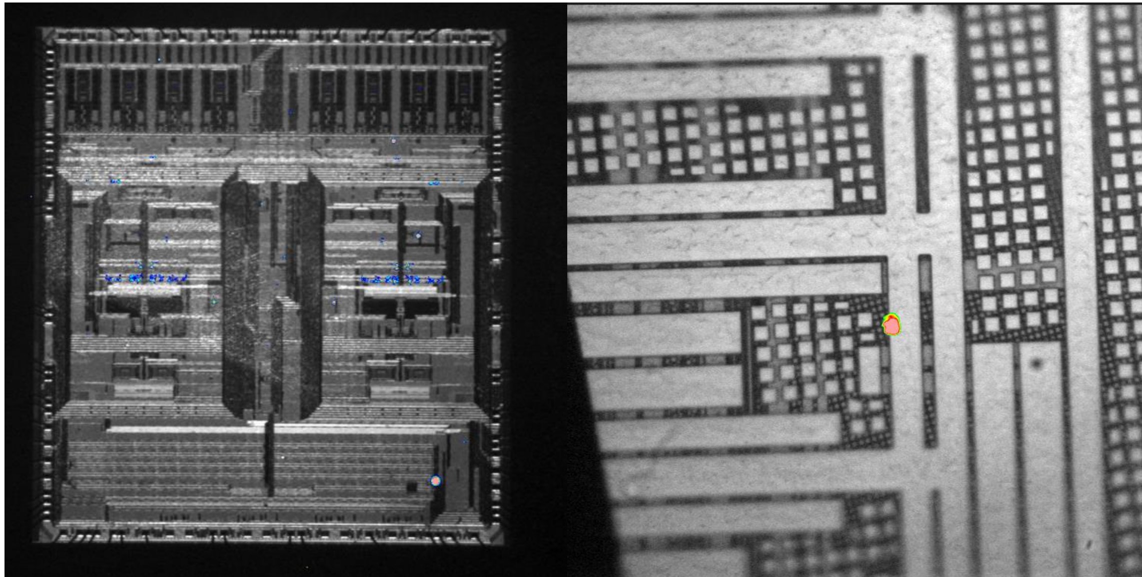


Figure 18: Hotspot images of ADS9818 during replicated latchup state from Phemos1000 at magnification 1× [Left] and 50× [Right].

ADS8168

Now, we test one of our main hypotheses whether we can assume that UV/PEM experimental method has a similar ADC performance behavior when irradiated with heavy ions. We postulate that the components that were subjected to replicated latchup from high energy photon irradiation observed in the images captured by the Phemos1000 system are the same parts within the circuit that experience SELs when exposed to heavy-ion radiation. This postulate is based on the premise that in this experiment by inducing a latchup state in ADC through the use of UV flashlamp; the Phemos1000 system has successfully identified and localized the areas within the circuit that underwent latchup replication. By correlating the observed hotspots and affected areas in the images with the circuit's behavior during high energy photons radiation exposure, we can hypothesize that these specific components are the ones that undergo SEL under such conditions. Further experimental tests and analyses are required to validate this postulate conclusively. By subjecting the identified components to additional radiation tests and monitoring their response, we can gather more data to support or refute the proposed hypothesis.

Device and Test Board Information

The ADS816x is a family of 16-bit, 8-channel, high precision successive approximation register (SAR) analog-to-digital converters (ADCs) operating from a single 5-V supply with a 1-MSPS (ADS8168), 500-kSPS (ADS8167), and 250-kSPS (ADS8166) total throughput. ADS8168 is packaged in a 32-pin plastic package as shown in Fig. 20. The ADS8168EVM evaluation module was used to evaluate the performance and characteristics of the ADS8168 under heavy-ions. Fig. 21 shows the top view of the evaluation board used for the radiation testing.

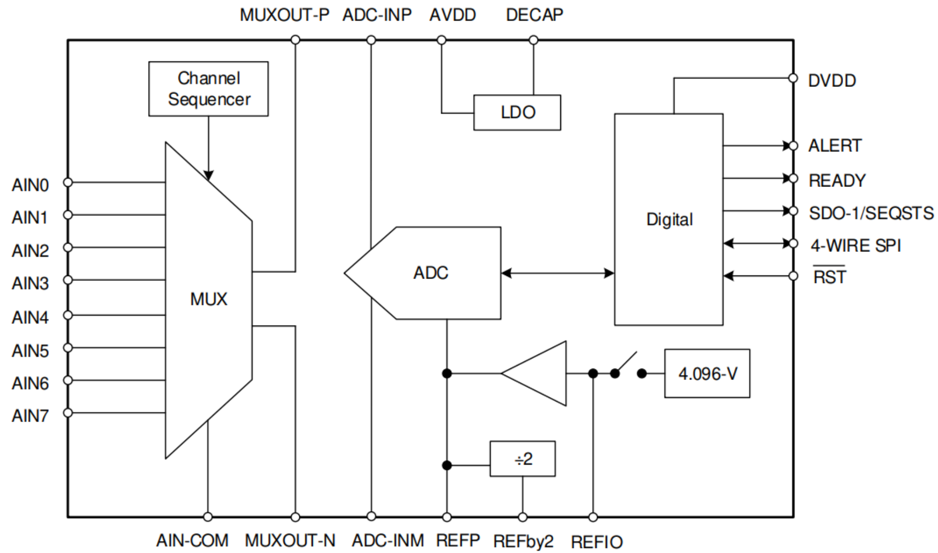


Figure 19: Functional block diagram of the ADS8168.

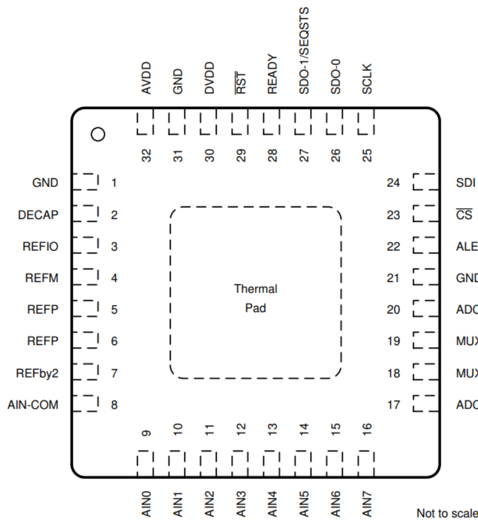


Figure 20: ADS8168 pin configuration.

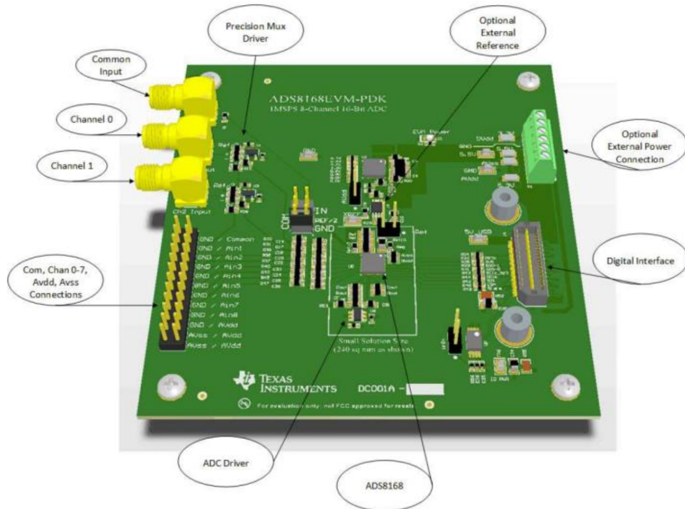


Figure 21: ADS8168EVM board top view.

Irradiation Facility and Setup

The heavy-ion SEE studies were conducted at the TAMU Cyclotron Radiation Effects Facility. At the fluxes used, ion beams had good flux stability and high irradiation uniformity over a 1 inch diameter circular cross-sectional area for the in-air station. Uniformity was achieved by magnetic defocusing. The flux of the beam was changed over a broad range spanning several

orders of magnitude. For the bulk of these studies, ion flux of 10^5 ions/cm^2−s were used to provide heavy-ion fluence of ≈10^7 ions/cm^2. For the experiments conducted for this device, silver isotope ions ^{109}Ag at angle of incidence of 0° for an LET_{EFF} of 48.2 MeV-cm^2/mg were used. The total kinetic energy of ^{109}Ag was 1.634 GeV (15 MeV/nucleon). Ion uniformity for these experiments was between 94% and 97%. Fig. 22 shows the ADS8168EVM test board used for the experiments at the TAMU facility. Although not visible in this photo, the beam port has a 1-mil Aramica window to allow in-air testing while maintaining the vacuum within the accelerator with only minor ion energy loss. The in-air gap between the device and the ion beam port window was maintained at 40 mm for all runs. The voltage supply for VA and VD was provided externally on the board, with the highest recommended voltage setting of 3.6 V. During the SEL characterization process, the device was heated using a heat gun and kept at 85 °C.

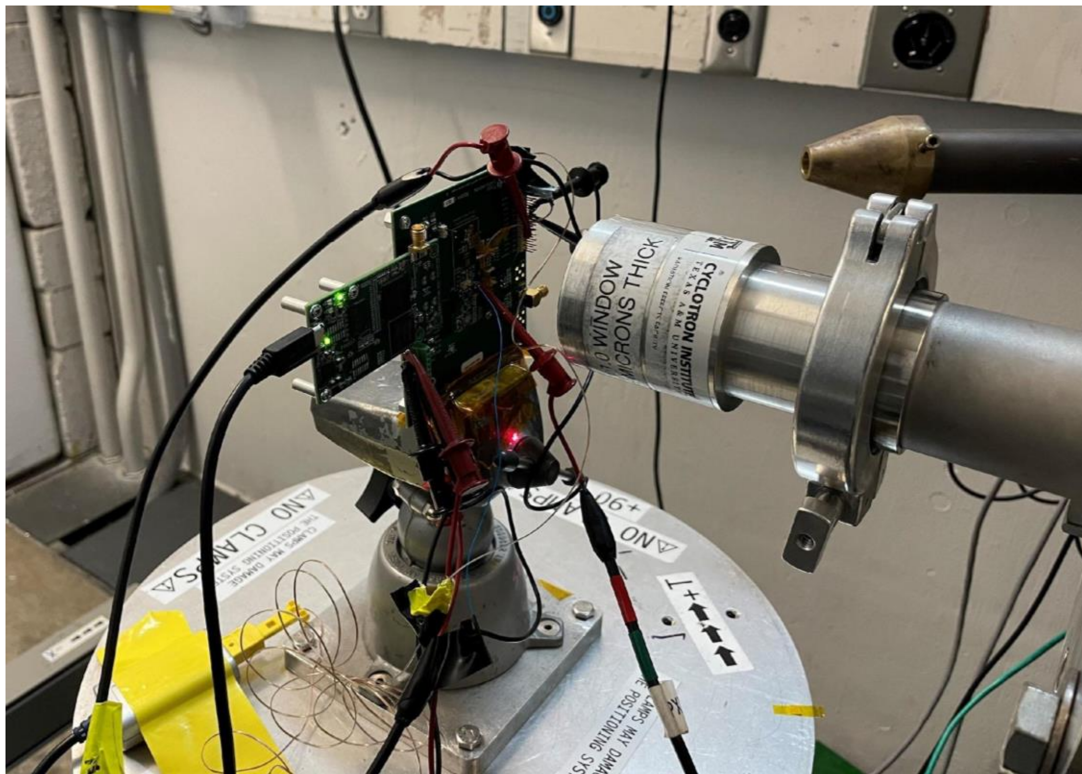
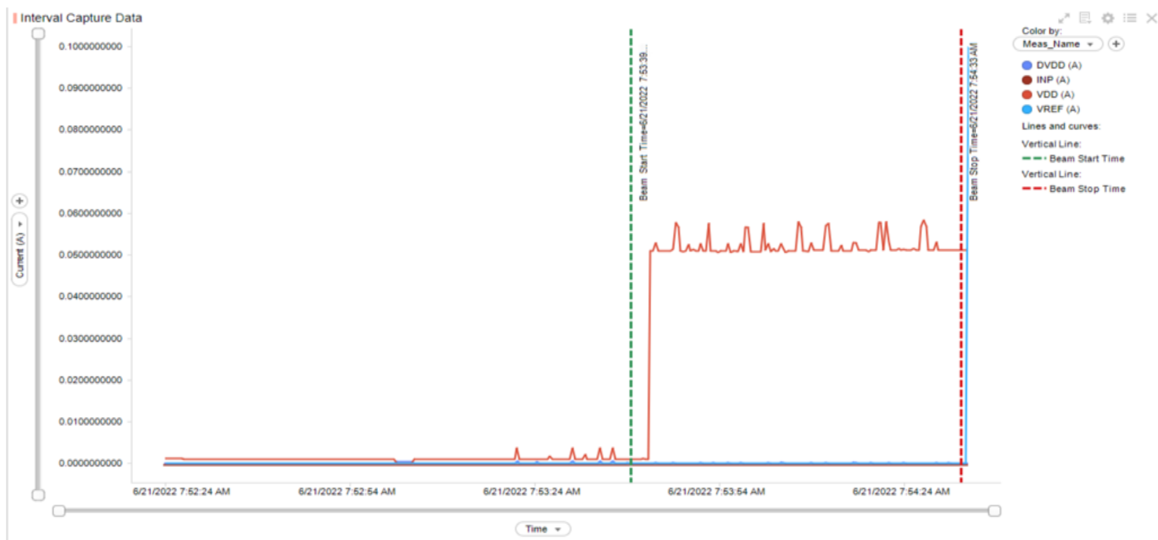


Figure 22: Photograph of the ADS8168EVM mounted in front of the heavy-ion beam exit port at the TAMU cyclotron.

ADS8168 *FIB1* SEL plot Run # 7 Ag with 0^0 Angle LET =48 Mev @ 85C



- AVDD and DVDD @ 3.6V This is FIB1 that disabled VREF. **SEL FAILED**

Figure 23: Current vs time (I vs t) data for Vs current during SEL Run #7.

Single-Event Latchup Results

Fig. 23 displays a plot of the current versus time for one of the runs. It is evident that upon the launch of the beam, indicated by the green dotted line, there is an immediate increase in current from AVDD up to 50 mA. Consequently, it has been determined that the ADS8168 does not meet the necessary criteria to be used in space applications.

PEM Failure Analysis and Discussion

During the second part of the experiment we used the same ADC ADS8168 for failure analysis by the use of UV flashlight and PEM tool. The voltage supply for VA and VD was provided externally on board, with the highest recommended voltage setting of 5.5 V, however the power supply currents were 24 mA and 5 mA respectively, which doesn't fall under datasheet's recommended electrical characteristics. Our assumption is that the device was damaged by heavy

ions at TAMU. This further strengthens our initial hypothesis that heavy ion and PEM are complementary and that the images below capture exactly the same locations that latched-up at TAMU. During failure analysis, the device was tested at room temperature. Table 3 illustrates many latchups at once. Additionally, Fig. 24 and Fig. 25 shows images of the hot spots, providing more details into chip internal areas that are susceptible to latchup.

Table 3: Power Supply currents during Latch-up replication test.

Device Status	AVDD (5.5V)	DVDD (5.5V)
Power Up Current	24mA	5mA
Post Flash	25.8mA	7mA

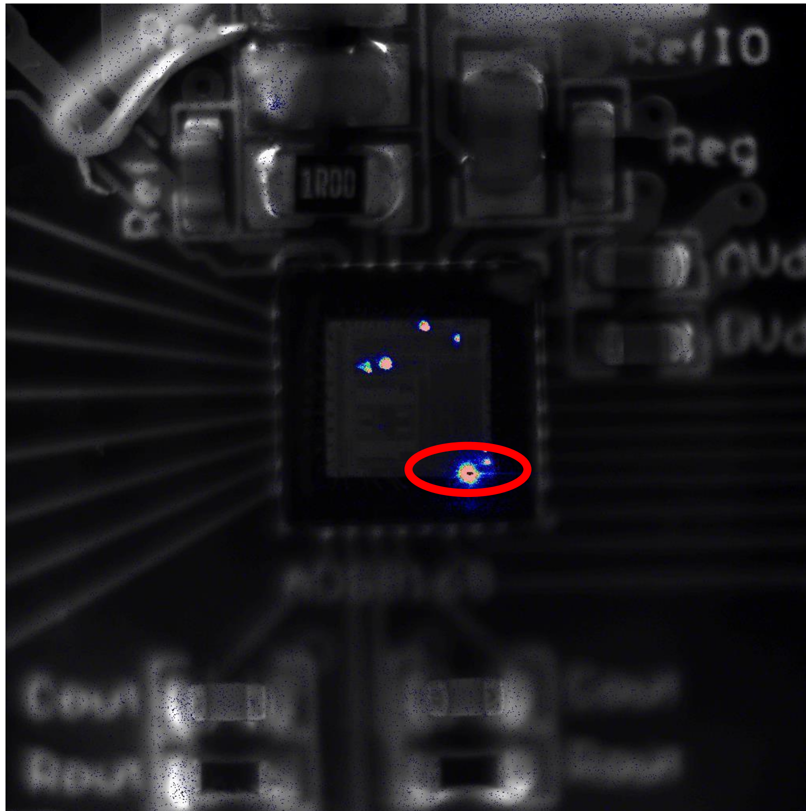


Figure 24: [x1] Hotspot image of ADS8168 during replicated latchup state from Phemos1000.

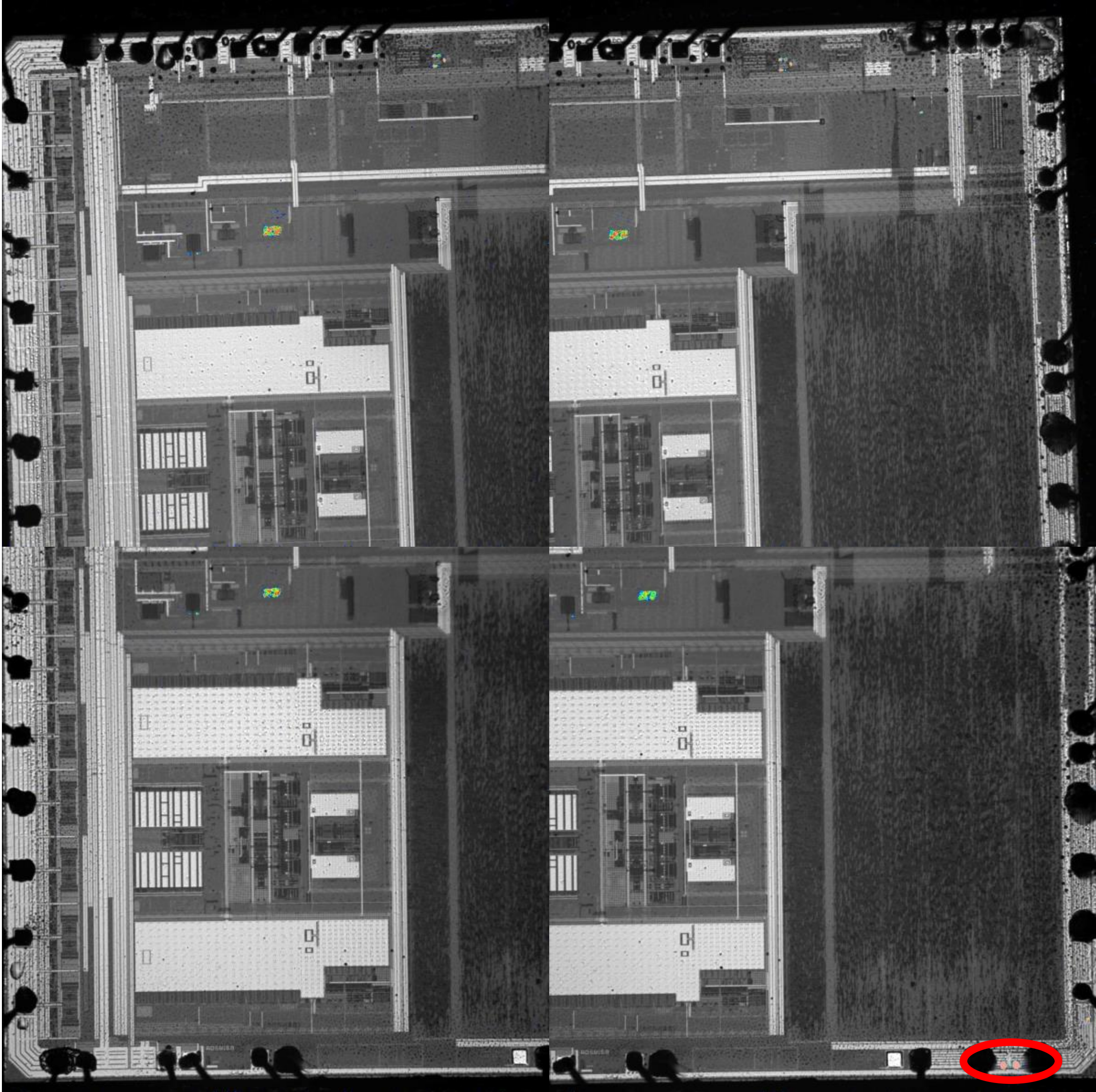


Figure 25: [x5] Hotspot images of ADS8168 during replicated latchup state from Phemos1000.

Summarizing, the tests at TAMU involved heavy-ion exposure, which induced SEL in the ADC and subsequently caused a functional failure. Based on the performance of the device, it was assumed that it is indicative of hard error SEL occurrence, possibility that SEL after-effect lead to more serious SEE hard errors like Single Event Gate Rupture or Single Event Burnout as electrical characteristics of the ADS8168 were incorrect from the get-go in PEM analysis. The PEM tool was used to identify specific sections of the ADC that were latching during the prior tests at

TAMU. Since the exact topology and layout of the chip is unknown, it is difficult to pinpoint the exact components that are latched-up. However, based on the image provided by the Phemos1000 system, it can be inferred that one of the latchup events occurred in the lower right corner of the chip which is highlighted in red circle. This location is likely in close proximity to the input/output (I/O) circuitry of the ADC or near the power lines connecting to the power supply (AVDD). This result can serve as a proof of our complementary hypothesis, since during the initial tests at TAMU, when irradiated with heavy particles, the AVDD current got to an elevated state of 50 mA; by correlating this with the second PEM tests when AVDD current state reached 25.8 mA. The biggest hotspot located in the lower right corner of the chip suggested that latchup damaged the power supply lines.

SUMMARY & CONCLUSION

In this study, we sought to gain a comprehensive understanding of single event latch-up (SEL) phenomenon in off-the-shelf integrated circuit (IC) products by TI, specifically focusing on analog-to-digital converters (ADCs). SEL occurrences in ICs have long been a critical concern for electronic systems used in harsh environments, particularly in space applications, where the effects of energetic particles can result in disastrous consequences for electronic devices. To this end, we explored the reasons behind the occurrence of SELs, their impact on circuit behavior, and failure localization within ICs where SELs occur. To conduct our investigation, we employed a series of rigorous experimental tests on multiple ADCs that were provided by Texas Instruments, which were subjected to heavy-ion irradiation and semi-invasive ultraviolet (UV) flashlight attacks. The ADCs chosen for the study were the ADS131M08, a 24-bit delta-sigma (ΔΣ) ADC; the ADS9818, a high-speed, 18-bit SAR ADC; and the ADS8168, a 16-bit SAR ADC. These ADCs were selected, with the aim of providing an understanding of the SEL phenomenon. The heavy-ion irradiation tests were conducted at the MSU FRIB facility for the ADS131M08 and at the TAMU facility for the ADS8168. The devices were exposed to heavy ions with LET_{EFF} values of 75 MeV-cm^2/mg and 48 MeV-cm^2/mg, respectively, and at a fluence of 1×10^7 ions/cm^2.

By analyzing the behavior of the Ics during an SEL event, we found that the occurrence of an SEL could result in increased current flow, potential component damage, and the risk of malfunction or failure. Through a series of experiments involving heavy-ion irradiation and semi-invasive UV flashlight attacks, we were able to shed light on the SEL performance and localize failure sections in the ADCs. Our results demonstrated that both the ADS131M08 and the ADS8168 devices exhibited SEL failures under certain conditions, with the assumption that one of the devices was destroyed due to a high-current state. Furthermore, we explored the use of semi-

invasive UV flashlight attacks in conjunction with PEM for localizing and identifying the specific components that are susceptible to SELs. By replicating a latch-up state through the use of high-energy photons directed at the decapped chip of the circuit, we were able to create controlled conditions that facilitated the examination of SEL-prone elements without necessitating power-cycling of the device and without the need to use the expensive cyclotron facilities. This approach proved an invaluable methodology in observing hotspots within the circuit and identifying internal structure components that could potentially be susceptible to single event latch-up events.

Lastly, we investigated the possibility of correlating the observed hotspots and affected areas in the images captured by the Phemos 1000 system with the circuit's behavior during heavy-ion radiation exposure. By hypothesizing that these specific components are the ones that undergo SEL under such conditions, we postulated that the components observed in the images are the same parts within the circuit that experience SELs when exposed to heavy-ion radiation. Although our results are promising, further experimental tests and analyses are required to validate this postulate conclusively. By subjecting the identified components to additional radiation tests and monitoring their response, we can gather more data to support or refute the hypothesis. The results of this study highlight the significance of understanding the SEL phenomenon in integrated circuits and the potential consequences of such events on the performance and reliability of electronic devices, particularly in space applications. By utilizing a combination of heavy-ion irradiation, semi-invasive UV flashlight attacks, and PEM techniques, we have gained valuable insights into the behavior of integrated circuits during SEL events, and localization failure within an IC where SEL is most likely to occur. Moreover, our study demonstrates the importance of identifying and localizing failure-prone components within integrated circuits to ensure the robustness and reliability of electronic devices in demanding environments.

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APPENDIX: SEL CROSS SECTION CALCULATION FOR ADS131M08

1) An integrated circuit with a total exposed area of 2×4 mm^2. Convert the exposed area to square centimeters as 0.08 cm^2;

2) Total number of latch-up events: During all three runs there were a total of 3 latch-up events;

3) Total fluence: The device was exposed to a fluence of 1×10^7 ions/cm^2 in each run, and there were 3 runs. The total fluence experienced by the device was then Total fluence = (Fluence per run)×(Number of runs) = 3×10^7 ions/cm^2;

4) Latch-up probability: Calculate the probability of a latch-up event per unit fluence by dividing the number of latch-up events by the total fluence as Probability = (Number of latch-up events) / (Total fluence) = 3/(3×10^7 ions/cm^2) = 1×10^{-7} latch-up events per ion/cm^2;

5) SEL cross-section: Calculate the SEL cross-section by dividing the latch-up probability by the exposed area of the device as SEL cross-section = (Latch-up probability) / (Exposed area) = (1×10^{-7} latch-up events per ion/cm^2) / (0.08 cm^2) = 1.25×10^{-6} cm^2.

In this case, the calculated SEL cross-section is 1.25×10^{-6} cm^2. This value represents the likelihood of a latch-up event occurring in the device when exposed to the specific radiation source with a fluence of 1×10^7 ions/cm^2 per run.

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